PAPER

Dual Evanescently Coupled Waveguide Photodiodes with High Reliability for over 40-Gbps Optical Communication Systems

Kazuhiro SHIBA[†a)], ***Member***, **Yasuyuki SUZUKI**[††], ***Senior Member***, **Sawaki WATANABE**[†††*], **Tadayuki CHIKUMA**[†], ***Nonmembers***, **Takeshi TAKEUCHI**[†], ***and*** **Kikuo MAKITA**[†**], ***Members***

SUMMARY For over 40-Gbps optical communication systems, phase coded modulation formats, like differential phase shift keying (DPSK) and quadrature phase shift keying (QPSK), are very important for signal frequency efficiency and long-reach transmission. In such systems, differential receivers which regenerate phase signals are key components. Dual Photo Diodes (dual PDs) are key semiconductor devices which determine the receiver performance. Each PD of the dual PDs should realize high speed performance, high responsibility and high input power operation capability. Highly symmetrical characteristics between the two PDs should be also realized, thus the dual PDs are desired to be monolithically integrated to one chip. In this paper, we describe the design, fabrication, characteristics and reliability of monolithically integrated dual evanescently coupled waveguide photodiodes (EC-WG-PDs) for the purpose described above. The structure of the EC-WG-PDs offers the attractive advantages of high speed performance, high responsivity and high input power operation. Furthermore, their fabrication process is suitable for the integration of two PDs on one ship. First, the optimization was done for high products of 3-dB bandwidth and responsivity for 43-Gbps DPSK receivers. Excellent characteristics (50 GHz bandwidth with a responsivity of 0.95 A/W), and high reliability were demonstrated. The other type of optimization was done for ultra high speed operation up to 100-Gbps. The fabricated PDs exhibited the 3 dB-bandwidth of 80 GHz with a responsivity of 0.25 A/W. Furthermore, 43-Gbps RZ-DPSK receivers including the dual EC-WG-PDs based on the former optimization and differential transimpedance amplifiers (TIAs) newly developed for the purpose were also presented. Clear and symmetrical eye openings were observed for both ports. The OSNR characteristics exhibited 14.3 dB at a bit error rate of 10^{-3} that is able to be recovery with FEC. These performances are enough for practical use in 43-Gbps RZ-DPSK systems.

key words: *100-Gbps, 40-Gbps, differential phase shift-keying (DPSK), reliability, waveguide photodiode*

1. Introduction

Over 40-Gbps optical communication systems are required by a demand of high throughput multimedia service networks and future large scale sensor networks. In those communication systems, advanced optical modulation formats like differential phase shift keying (DPSK) and quadrature phase shift keying (QPSK) are needed because of their high frequency efficiency. These performances allow for smooth upgrade from 10-Gbps to over 40-Gbps transmission speed without interrupting the existing service in practical networks. Moreover, these phase coded modulation formats give the larger tolerance to fiber nonlinearities than on-off keying. In such systems, differential receivers which regenerate phase signals are key components. Dual PDs are key devices which determine the receiver performance [1]–[3]. They can receive the balanced optical signals simply by two input ports.

Required specifications for dual PDs are high speed performance, high responsivity, high reliability, and highly symmetrical characteristics between the two PDs. For the symmetry, monolithic integration of two PDs is essential in order to ensure the symmetry of the structure and the dimension between the two PDs. The integration is also effective for the reduction of the receiver size and cost. Robustness against high input power is also required for the PDs, because an erbium doped fiber amplifier (EDFA) must be deployed in the transmission line.

Trade-off between the speed and the responsivity is also a key issue. In high speed photodiodes, thinner absorption layers are usually desired to reduce the carrier transition time. However their responsivity would be degraded. In order to overcome the trade-off, waveguide photodiodes (WG-PDs) have been intensively investigated [4]–[10]. However, in WG-PDs, the input light is directly focused on the edge of the absorption layer, thereby causing a catastrophic damage under high input power operation.

Evanescently coupled waveguide photodiodes (EC-WG-PDs) have very attractive features to satisfy the requirements described above. We have previously reported that EC-WG-PDs exhibited high speed performance, high responsivity and high input power operation capability [11]. Because their responsivity mainly depends on the absorption length, the absorption layer can be thin for high speed operation without deteriorating responsivity. Moreover, the input light gradually couples into absorption layer, and then the mechanism is suitable for high input power operation. Furthermore, their fabrication process is suitable for the integration of two PDs because closely located PDs can be precisely formed by a dry-etching [12].

In this paper, the details of design, fabrication, characteristics, and reliability of dual EC-WG-PDs are described systematically. The feasibility of high speed performance and high responsivity were theoretically investigated, showing the PD designs for the two-types of applications. The

Manuscript received July 5, 2010.

[†]The authors are with Fiber Optics Device Division, NEC Corp., Abiko-shi, 270-1198 Japan.

[††]The author is with System Platform Res. Labs., NEC Corp., Kawasaki-shi, 211-8666 Japan.

[†††]The author is with Nanoelectronics Res. Labs., NEC Corp., Otsu-shi, 520-0833 Japan.

[*]Presently, with NEDO.

[**]Presently, with AIST.

a) E-mail: k-shiba@cd.jp.nec.com

DOI: 10.1587/transele.E93.C.1655

maximum 3-dB bandwidth and responsivity for different structures were accurately clarified by calculating the carrier transit time and a beam propagation method (BPM). One design (type-A) was optimized for the use of 43-Gbps DPSK receivers, and the other (type-B) for the use of even higher-speed receivers. For the type-A PDs, 50-GHz bandwidth with the responsivity of 0.95 A/W was experimentally obtained. For the type-B PDs, 3-dB bandwidth of 80 GHz with a responsivity of 0.25 A/W was experimentally obtained. The reliability was also reported for the PDs with the type-A design. The failure rate of better than 88 FIT at 25°C for a confidence level of 60% was demonstrated. 43-Gbps RZ-DPSK receivers including the type-A dual EC-WG-PDs and a newly developed differential transimpedance amplifier (TIA) were presented. A 3-dB bandwidth of 42 GHz, a high transimpedance gain of 58 dBΩ and clear and symmetrical eye-opening of each output port were obtained. The OSNR characteristics exhibited 14.3 dB at a bit error rate of 10^{-3} that is able to be recovery with FEC.

This paper is constructed as follows. In Sect. 2, the details of design and fabrication of the dual EC-WG-PDs are described. In Sect. 3, experimental results on the fabricated dual EC-WG-PDs with designs type-A and B are shown. In Sect. 4, high reliability of the type-A EC-WG-PDs was demonstrated. In Sect. 5, 43-Gbps RZ-DPSK receivers including the dual EC-WG-PDs and a newly developed TIA are presented. The summary of the paper is given in Sect. 6.

2. Fabrication and Design of EC-WG-PDs

2.1 Fabrication of EC-WG-PDs

A schematic structure of a fabricated dual EC-WG-PD and a refractive index profile of the graded-index waveguide layer are shown in Fig. 1 and Fig. 2, respectively. As shown in Fig. 1, two EC-WG-PDs are monolithically integrated on one chip, and the dimension is identical to each other PDs with 4 μm width (W_{PD} in Fig. 1). The EC-WG-PD consists of an input region and a PD region. All the semiconductor layers were grown using gas-source molecular beam epitaxy on a semi-insulating (S.I.) InP substrate. A spot size converter with 7 μm width at the facet (W_{facet} in Fig. 1) was introduced in order to increase the alignment tolerance. An input region was as short as 20 μm long (L_{input} in Fig. 1), considering optical propagation loss. As shown in Fig. 2, the graded-index waveguide layer consists of some pairs of InP and InGaAsP with the compositional wavelength of 1.2 μm. The layer thickness ratio of InGaAsP to InP gradually increases from the substrate to the absorption layer. Due to the index profile, effective refractive index increases toward the absorption layer. After propagating in the input region, the light is gradually coupled into InGaAs absorption layer to be absorbed. Therefore photo-generated carriers are distributed along the waveguide. This allows for more robust operation than conventional waveguide PIN-PDs under high input power operation.

Figure 3 shows the scanning electron microscope photograph of the fabricated device. Smooth and vertical surface on the waveguide side was successfully formed. Dry etching technique was introduced to precisely form mesa structures, which allows identical characteristics of two PIN-PDs and reproducibility. However, dry etching technique could induce damage in semiconductors devices, which results in high dark current and less reliability. The inductively coupled plasma (ICP) dry etching technique was introduced. Separate control on ion density and bias voltage of the plasma in ICP allows for highly precise and very low damage etching for compound semiconductors [13]. Deep dry etching was performed to the S.I. InP substrate in order to isolate each PD electrically and optically. The top surface was covered with a SiNx film deposited using plasma-enhanced chemical vapor deposition (P-CVD) after ICP dry etching process. An anti-reflection coating was also formed

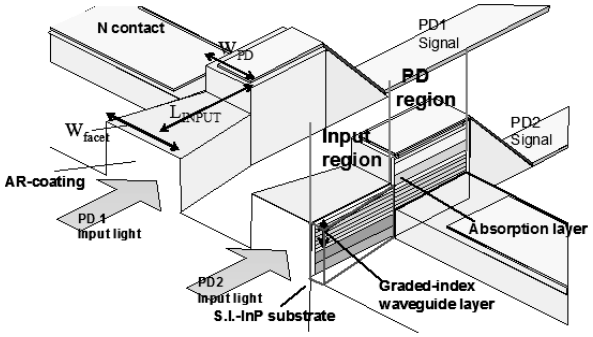

Fig. 1 Schematic structure of an EC-WG-PD.

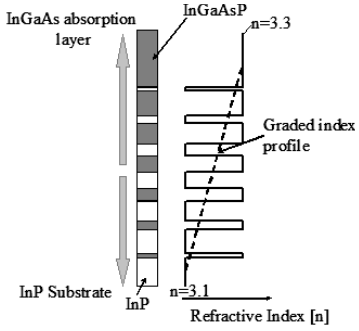

Fig. 2 Refractive index profile of graded-index waveguide layer.

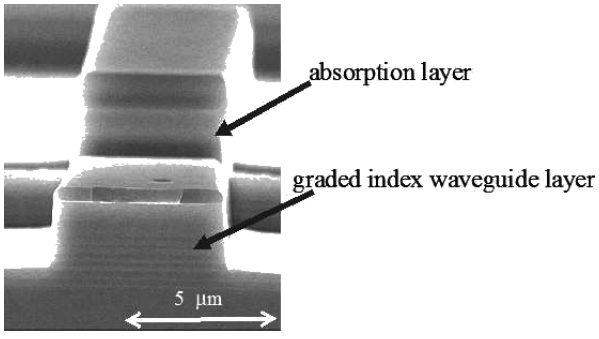

Fig. 3 Scanning electron microscope photograph.

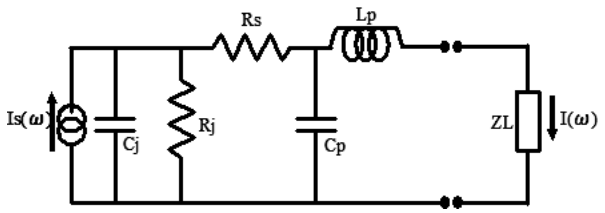

Fig. 4 Equivalent circuit model of the EC-WG-PDs.

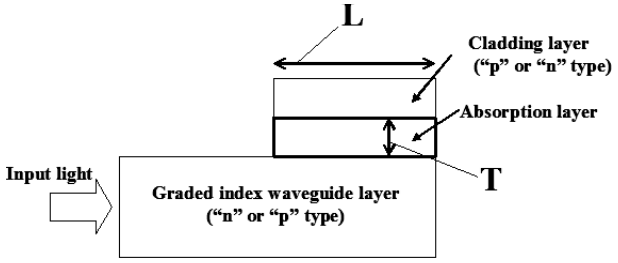

Fig. 5 The EC-WG-PD structure model for calculation.

on the cleaved facet of the input waveguide using the P-CVD.

2.2 Design of an Absorption Layer

Figure 4 shows an equivalent circuit model of the EC-WG-PDs, where Is(ω) is an equivalent current which comes from a photo-current in parallel to pn junction capacitance Cj and junction resistance Rj. Rs is a device series resistance, and Cp and Lp are a capacitance and a inductance of the electrode, respectively. Cj and Rs depends on their area size. Rj was very large and its impact can be neglected. Cp and Lp were assumed to be 20 fF and 100 pH, respectively. Here, load resistance ZL set to be 50 Ω. The effect of the carrier transit time through the absorption layer gives an impact on I(ω). It must be designed carefully in order to achieve high speed performance by considering the carrier transit time rigorously. Figure 5 shows a structure of the EC-WG-PD which is used in the calculation. Is(ω) is given by an integral of electron current density $J_n(x,\omega)$ and hole current density $J_p(x,\omega)$ over the total absorption layer thickness of T [14].

$$Is(\omega) = \frac{1}{T}\int_0^d (J_n(x,\omega) + J_p(x,\omega))dx \tag{1}$$

$J_n(x,\omega)$ and $J_p(x,\omega)$ are given by the carrier transport equation in frequency domain written as [15]

$$\frac{i\omega}{v_p}J_p(x,\omega) = -\frac{dJ_p(x,\omega)}{dx} + G(x,\omega) \tag{2}$$

$$\frac{i\omega}{v_n}J_n(x,\omega) = \frac{dJ_n(x,\omega)}{dx} + G(x,\omega) \tag{3}$$

where v_n and v_p are the electron and hole velocities, respectively. $G(x,\omega)$ is a carrier generation term, which is a function of the position of generated electron-hole pairs. The frequency response of carrier transition is calculated by the matrix algebra which was developed by James N. Hollenhorst

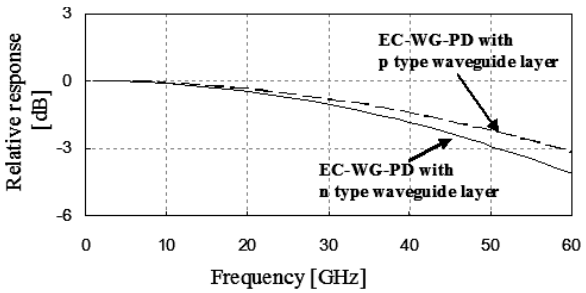

Fig. 6 Calculated frequency response dependent on doping type in waveguide layer.

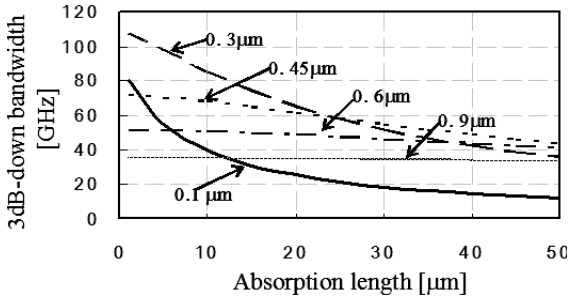

Fig. 7 Simulation results of 3-dB bandwidth as a function of absorption length. The inset values indicate the absorption thickness.

[16]. Figure 6 shows the simulation results of the frequency response of Is(ω) for the EC-WG-PDs with n-type doped waveguide layer and with p-type doped waveguide layer. For both structures, the absorption layer thickness was set to be 0.6 μm. Here only carrier transit time was taken into account. As shown in Fig. 6, 3-dB bandwidth for the EC-WG-PD with n-type waveguide exhibits 50 GHz, which is 7 GHz smaller than that with p-type waveguide. In the EC-WG-PDs, light is absorbed in the absorption layer only near the waveguide layer; therefore the carriers must run through the whole absorption layer. In the case of the p-type waveguide device, electron must run to the other n-type side. On the other hand, in the case of n-type waveguide, hole runs vice versa. Electrons run usually faster than holes in an InGaAs layer, and moreover in this model in Fig. 6, the speed was limited only by the carrier transit time. Therefore, a p-type waveguide is preferable. However, the device was fabricated with n-type waveguide layer in this work. Because the series resistance in the EC-WG-PDs with p-type doped waveguide layer could be lager than that with n-type doped waveguide layer. This is because the sheet resistance in the waveguide layer impacts the series resistance of the device as shown in Fig. 1. Furthermore, the effect of free carrier absorption and inter valence band absorption are not negligible in the p-type doping semiconductors, which would results in less responsivity.

Simulated 3-dB bandwidth curves as a function of the absorption length (L in Fig. 5) are shown in Fig. 7. The different absorption layer thicknesses from 0.1 μm to 0.9 μm (T in Fig. 5) were calculated. Here the RC time constant was also taken into account. As a result, a 3-dB bandwidth

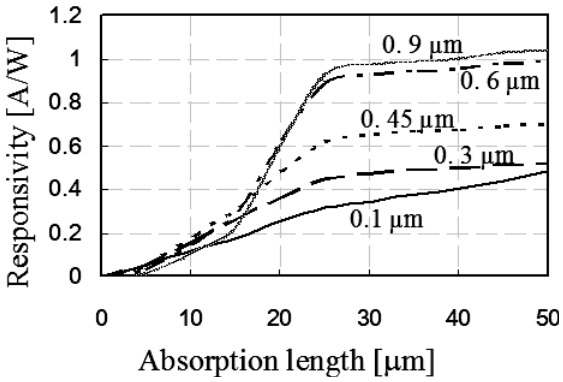

Fig. 8 Simulation results of responsivity as a function of absorption length. The inset values indicate the absorption thickness.

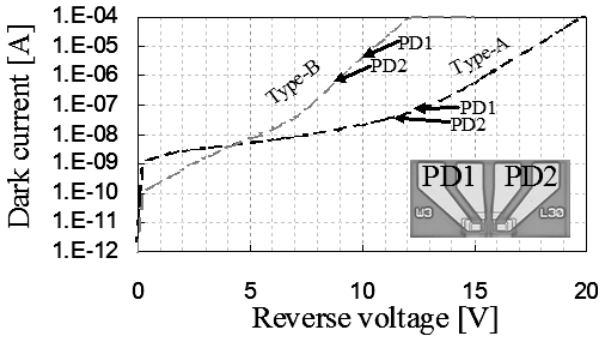

Fig. 9 Measured dark current characteristics versus reveres voltage in PD1 and PD2 for type-A and type-B.

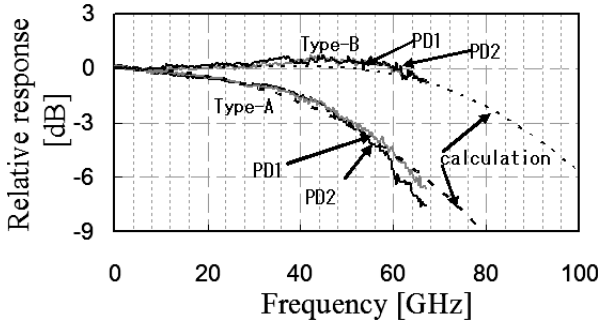

Fig. 10 Measured frequency responses and fitted curves of type-A and type-B.

decreases as a capacitance increases for a longer absorption region or absorption layer especially thinner than 0.3 μm. This indicates that the 3-dB bandwidth is limited by the RC time constant, where the carrier transition time is not a limitation factor for longer absorption length and thinner absorption thickness. On the other hand, for the device with the absorption layer thicker than 0.6 μm, a 3-dB bandwidth shows less dependence on the absorption length, thus the carrier transition time turns to be dominant, where the increase of the capacitance can be neglected. Responsivity curves without coupling loss at 1.55 μm as a function of absorption length calculated by BPM are shown in Fig. 8. Responsivity is saturated for thicker absorption layer than 0.6 μm. Moreover, responsivity increases up to 30 μm absorption length, and becomes saturated. For an absorption layer thinner than 0.3 μm, the input light radiates to p-InP cladding layer and InP substrate before it is absorbed in InGaAs absorption layer. This causes less responsivity even with longer absorption layer.

In this work, based on the simulation results above, two types (type-A and type-B) of EC-WG-PDs were fabricated. Type-A with an absorption layer thickness of 0.6 μm and a length of 30 μm was designed for high products of 3-dB bandwidth and responsivity for 43-Gbps DPSK receivers and type-B with an absorption thickness of 0.3 μm and a length of 10 μm was designed for ultra high speed operation up to 100-Gbps.

3. Device Characteristics

Experimental results on typical dark current versus reverse voltage characteristics of PD1 and PD2 for both type-A (0.6 μm absorption thickness, 30 μm absorption length) and type-B (0.3 μm absorption thickness, 10 μm absorption length) are shown in Fig. 9. For both types, both PDs show identical I-V characteristics. The measured dark current was less than 5 nA at 3 V bias for both types. As shown in Fig. 9, the slopes of the I-V curves were changed around 13 V bias for type-A and also around 7 V bias for type-B. This implies that the leakage current on the mesa surface was dominant at lower bias voltage and at higher bias voltage the tunneling current through InGaAs absorption layer turned to be dominant. Although the turning points of the slopes seem to be different for both types, it actually depends on electric field magnitude. In this experiment, it was 200 kV/cm. The measured typical capacitances were 62 fF for type-A and 34 fF for type-B at 3 V. The capacitance variation of both PD1 and PD2 was within 5%, which was estimated from 76 samples with type-A. Therefore the variation of 3-dB bandwidth can be within 3%, which was derived from the slope of a 0.6 μm curve in Fig. 7. Measured responsivity including fiber coupling loss at 1.55 μm was 0.95 A/W for type-A, and that was 0.25 A/W for type-B. For practical use, fiber alignment tolerance must be also considered. The measured misalignment tolerance for 1-dB extra coupling loss was ±2.5-μm for horizontal axis and ±1-μm for vertical. An optical fiber with a mode diameter of 3.0 μm was used in this measurement. This wide tolerance for horizontal axis is due to the spot size converter in Fig. 1.

Figure 10 shows the frequency response at 1.55 μm wavelength, where input power was 0 dBm and the operation bias was 3 V for both type-A and type-B. The solid lines are experimental results which were measured by using an optical component analyzer. The dotted lines are simulation results. PD1 and PD2 show almost identical frequency responses. For type-A, the measured 3-dB bandwidth was 50 GHz, and it was limited mainly by the carrier transition time in the absorption layer. Moreover, a 3-dB bandwidth over 40 GHz was achieved with a wide input power

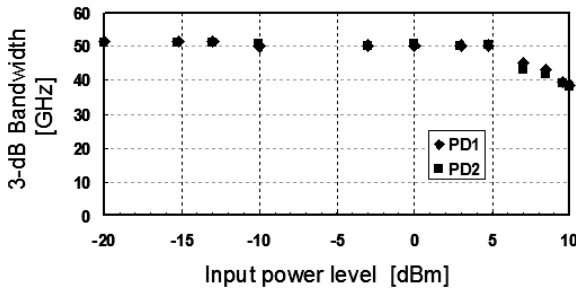

Fig. 11 3-dB bandwidth of type-A as a function of input power level.

range from −20 to +8.4 dBm as shown in Fig. 11. Type-B shows a flat frequency response up to 60 GHz because of its low capacitance and short carrier transit time. The measured frequency response shows good agreement with a fitted curve up to 67 GHz. Although the frequency response over 67 GHz was not measured due to the setup limit, the fitted curve of type-B shows a 3-dB bandwidth over 80 GHz.

4. Reliability

In this section, the screening and long-term accelerating test for the type-A which becomes key component for 43-Gbps DPSK receivers are shown. Before a long-term accelerating test, a screening test was carried out for 24 hours. The condition of screening test was done at a temperature of 120°C and a bias voltage of −6 V without input light. After that, long term accelerating test was conducted at a temperature of 175°C and a constant bias voltage of −6 V. There were 11 devices tested and the transition of dark current was measured. The condition of the bias voltage of −6 V was twice as severe as that of a practical operation. The variation of the dark current transition at room temperature during screening and long-term accelerated test is shown in Fig. 12. The test was interrupted to measure the dark current at room temperature. The life time was estimated to be more than 1×10^5 hours at 85°C by using activation energy of 0.35 eV. This value of 0.35 eV is recommended by telcordia for the random failure mechanism in photodiodes [17]. The estimated failure rate is 88 FIT at 25°C for a confidence level of 60%. Because practical operation condition is more relaxing than the aging test, FIT can be better than the above estimation. Figure 12 also shows that the dark current of all samples increased during the screening test. This change of dark current is due to the increased leakage paths of mesa surface between SiN files and InGaAs semiconductor layer [18], [19]. Above 10000 hours, the dark current showed still a very low value less than 20 nA. Over 40-Gbps systems the dark current below 100 nA can be neglected for the receiver performance. To conclude, high reliability of dry-etched dual EC-WG-PDs was successfully demonstrated.

5. Receiver Module Characteristics

A 43-Gbps differential receiver which includes a dual EC-WG-PD of type-A and a differential TIA based on InP-HBT

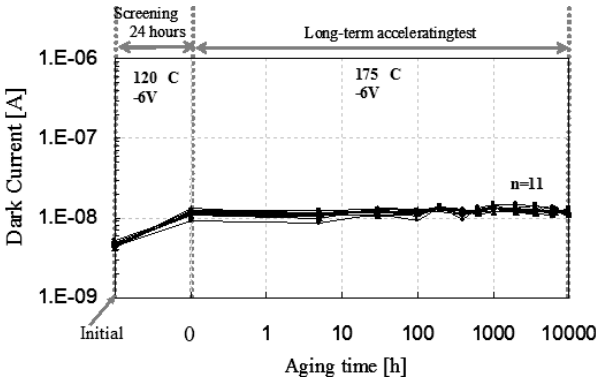

Fig. 12 Variation of dark current transition.

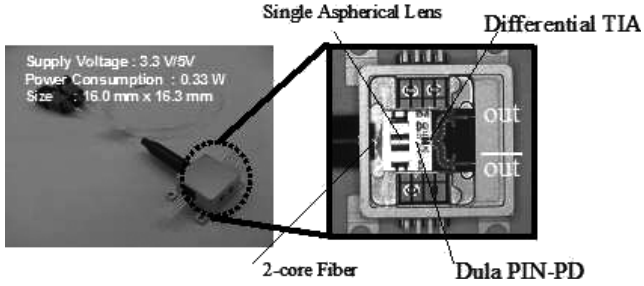

Fig. 13 Photographs of the fabricated differential receiver module with its inside view.

process technology was developed [20]. Figure 13 shows photographs of the differential receiver module with its inside view. Typical supply voltage and power consumption were 3.3 V/5 V and 0.33 W, respectively. The dimension of the package was as small as 16.0 mm × 16.3 mm. The layout of the module was designed symmetrically to achieve balanced signal phase adjustment. The module had balanced optical inputs and differential electrical outputs with GPPO connectors. The TIA consisted of 3 stages; a differential transimpedance, a differential AMP gain and an output buffer stages. Cherry-Hooper architecture was introduced in the differential AMP stage to obtain a wide bandwidth. The layout of the TIA was also kept symmetric to equalize the delays for differential signals. The chip size was 1.25 mm × 1.25 mm. The 3-dB bandwidth was 42 GHz at the operation bias of 3.3 V. The feedback resistance was set to be 200 Ω and a 58-dBΩ transimpedance gain was obtained. The measured return loss was less than −10 dB in a frequency range from DC to 42 GHz. Figure 14 shows the frequency response of the receiver module. A 3-dB bandwidth of 42 GHz was obtained at an input optical power level of −3 dBm. Simultaneously a low electrical return loss from DC to 40 GHz was also obtained. Moreover, the frequency response curve shows symmetric characteristics. The output wave forms in back to back transmission experiment are shown in Fig. 15 when 43-Gbps RZ-DPSK optical signal was input with 1-bit delay interferometer. Clear and symmetrical eye openings were observed for both ports with 350-mVpp output voltage swings. These symmetrical characteristics are brought by

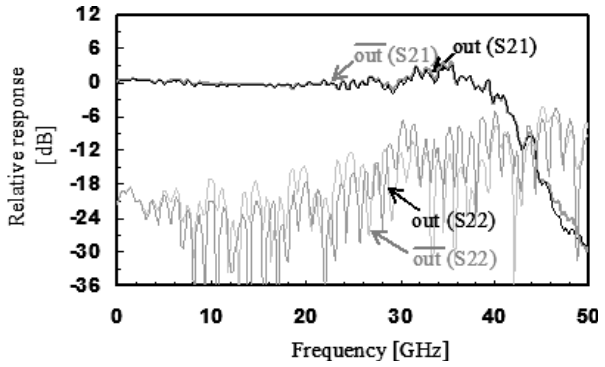

Fig. 14 Frequency response of the differential receiver module.

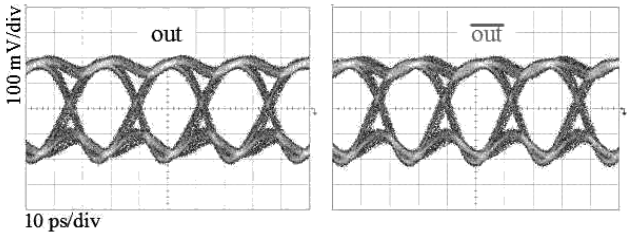

Fig. 15 Output waveform of the differential receiver module.

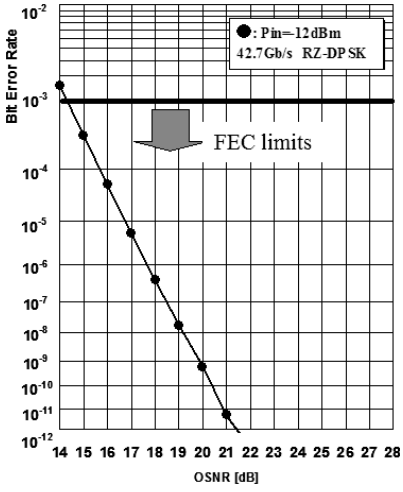

Fig. 16 OSNR characteristics at 42.7 Gbps RZ-DPSK.

monolithic integration of a dual PIN-PD and the symmetrical layout of the components and packaging.

Figure 16 shows the optical signal-to-noise ratio (OSNR) characteristics. The OSNR exhibited 14.3 dB at a bit error rate of 10^{-3}. This is enough to recover the signal with a forward error correction (FEC). From these characteristics above, differential receivers with a dual EC-WG-PD and a differential TIA have excellent performances for practical use in 43-Gbps DPSK systems.

6. Conclusions

The dual EC-WG-PDs were developed for DPSK and QPSK receivers. The feasibility of high speed performance and responsibility were theoretically investigated. Based on the simulation, two types of dual EC-WG-PDs were presented. First, the optimization was done for high products of 3-dB bandwidth and responsivity for 43-Gbps DPSK receivers. The fabricated dual EC-WG-PDs (type-A: 0.6 μm absorption thickness, 30 μm absorption length) exhibited the 3-dB bandwidth of 50 GHz with a responsivity of 0.95 A/W. The other type of optimization was done for ultra high speed operation up to 100-Gbps. The fabricated dual EC-WG-PDs (type-B: 0.3 μm absorption thickness, 10 μm absorption length) exhibited the 3-dB bandwidth of 80 GHz with a responsivity of 0.25 A/W. The reliability was also demonstrated for the type-A dual EC-WG-PDs. The failure rate of better than 88 FIT at 25°C for a confidence level of 60% was estimated. Moreover, 43-Gbps differential receivers which include a dual EC-WG-PD and a newly developed differential TIA were presented. Clear and symmetrical eye openings were observed for both ports when 43-Gbps RZ-DPSK optical signal was input with 1-bit delay interferometer. The OSNR characteristics exhibited 14.3 dB at a bit error rate of 10^{-3} that is able to be recovery with FEC. These performances indicate that the dual EC-WG-PDs are suitable for the use of 43-Gbps DPSK receivers.

Acknowledgments

The authors thank Dr. S. Tahara, Dr. H. Shimawaki, D. Inami, Dr. M. Nido from NEC Corporation and Prof. K. Kasahara from Ritumeikan University for their encouragement and helpful comments. We thank Dr. T. Nakata, Dr. T. Okamoto, T. Koga, K. Ohmori, T. Oami, and Dr. K. Sato from NEC Corporation for their fruitful discussions, and thank E. Mizuki, M. Miho and T. Yokomatsu from NEC Corporation for their technical support.

References

[1] A. Beling, "PIN photodiodes modules for 80 Gbit/s and beyond," Optical Fiber Comm., OFE1, 2006.
[2] A. Umbach, C. Schramm, G. Jacumeit, J.H. Sinsky, A. Asamiecki, A. Benz, and P. Paschke, "Integrated limiting balanced photoreceiver for 43 Gbit/s DPSK transmission," European Conf. on Optical Comm. (ECOC 2005), vol.3, pp.497–498, 2005.
[3] M. Nakaji, E. Ishimura, Y. Hanamaki, K. Shimomura, T. Aoyagi, and T. Ishikawa, "The balanced photodetector buried with semi-insulating InP," Lasers & Electro-Optics Society 2005, pp.460–461, 2005.
[4] J.E. Bowers and C.A. Burrus, "Ultrawide-band long-wavelength p-i-n phtodetectors," J. Lightwave Technol., vol.LT-5, no.10, pp.1339–1350, 1987.
[5] K. Makita, K. Shiba, T. Nakata, E. Mizuki, and S. Watanabe, "Recent advances in ultra-high-speed waveguide photodiodes for optical communication systems," IEICE Trans. Electron., vol.E92-C, no.7, pp.922–1928, July 2009.
[6] K. Kato, A. Kozen, Y. Muramoto, Y. Itaya, T. Nagatsuma, and M. Yaita, "110-GHz, 50%-efficiency mushroom-mesa waveguide p-i-n photodiode for a 1.55-μm wavelength," IEEE Photonics Technol. Lett., vol.6, no.6, pp.719–721, 1994.
[7] T. Takeuchi, T. Nakata, K. Fukuchi, K. Makita, and K. Taguchi, "A high-efficiency waveguide photodiode for 40-Gb/s optical recivers," IEICE Trans. Electron., vol.E82-C, no.8, pp.1502–1508, Aug. 1999.

[8] M. Nakaji, E Ishimura, Y. Hanamaki, T. Aoyagi, and Y. Mitsui, "Highly reliable wave-guide photodiode with wide bandwidth of 50 GHz at the low operation voltage of −1.5 V," Tech. Dig. Optical Fiber Commun. (OFC 2003), vol.1, pp.342–343, 2003.
[9] S. Shimizu, K. Shiba, T. Nakata, K. Kasahara, and K. Makita, "40 Gbit/s waveguide avalanche photodiode with p-type absorption layer and thin InAlAs multiplication layer," Electron. Lett., vol.43, no.8, pp.476–477, 2007.
[10] K. Shiba, T. Nakata, T. Takeuchi, T. Sasaki, and K. Makita, "10 Gbit/s asymmetric waveguide APD with high sensitivity of −30 dBm," Electron. Lett., vol.42, no.20, pp.1177–1178, 2006.
[11] T. Takeuchi, T. Nakata, K. Makita, and M. Yamaguchi, "High-speed, high-power and high efficiency photodiodes with evanescently coupled graded-index waveguide," Electron. Lett., vol.36, no.11, pp.972–973, 2000.
[12] S. Watanabe, K. Shiba, T. Okamoto, T. Chikuma, and K. Makita, "Dual-evanescently coupled waveguide photodiodes for ultra-high bit rate DPSK/DQPSK systems," Lasers & Electro-Optics Society 2007, pp.387–388, 2007.
[13] A. Matsutani, H. Ohtsuki, F. Koyama, and K. Iga, "Vertical and smooth etching of InP by Cl_2/Xe inductive coupled plasma," Jpn. J. Appl. Phys., vol.38, no.7, pp.4260–4261, 1999.
[14] W.T. Read, "A proposed high-frequency negative-resistance diode," Bell Syst. Tech. J., vol.37, pp.401–446, 1958.
[15] G. Lucovsky, R.F. Schwarz, and R.B. Emmons, "Transit-time considerations in p-i-n Diodes," J. Appl. Phys., vol.35, pp.622–628, 1964.
[16] J.N. Hollenhorst, "Frequency response theory for multilayer photodiodes," J. Lightwave Technol., vol.8, no.4, pp.531–537, 1990.
[17] Telcordia Technologies Generic Requirements, GR-468-CORE, Issue 2, Sept. 2004.
[18] I. Watanabe, M. Tsuji, H. Hayashi, K. Makita, and K. Taguchi, "Reliability of mesa-structure InAlGaAs-InAlAs superlattice avalanche photodiodes," IEEE Photonics Technol. Lett., vol.8, no.6, pp.824–826, 1996.
[19] T. Furuta, H. Fushimi, T. Yasui, Y. Muramoto, H. Kamioka, H. Mawatari, H. Fukano, T. Ishibashi, and H. Ito, "Highly reliable uni-traveling-carrier photodiodes for 40 Gbit/s optical transmission systems," Electron. Lett., vol.38, no.7, pp.332–334, 2002.
[20] T. Chikuma, K. Shiba, K. Makita, Y. Suzuki, T. Ohami, and N. Baba, "43-Gb/s differential receiver module for RZ-DPSK," European Conf. On Optical Commun. (ECOC 2008), P.1.14, 2008.

Kazuhiro Shiba was born in Tokushima, Japan, in 1970. He received his B.E and M.E. degrees from Kobe University and Osaka University in 1993 and 1995. He joined NEC Corporation in 1995. He was engaged in research and development on semiconductor lasers and highly sensitive photodiodes for optical communications in central laboratory in NEC. He is currently working on next generation optical modules in Fiber Optics Device Division in NEC. He received a Young Scientist Award for the Presentation of an Excellent Paper in 2004 from the Japan Society of Applied Physics (JSAP). He is a member of the Institute of Electronics, Information, and Communications Engineers of Japan.

Yasuyuki Suzuki was born in Toyama, Japan, in 1959. He received B.E. and M.S. degrees in engineering science and scientific technology, and a D.E. degree in electronic engineering from the University of Tsukuba, Ibaraki, Japan, in 1982, 1984 and 2000, respectively. In 1984, he jointed the Microelectronics Research Laboratories, NEC Corporation, Kawasaki, Japan, where he was engaged in the research and development of low-noise heterojunction FETs and high-speed heterojunction FET ICs. His current interests include in the research and development of high-speed ICs and high-speed optical transmission systems. He is also a Visiting Professor with the University of Electro-Communications, Tokyo, Japan.

Sawaki Watanabe received B.E. and M.E. degrees from the Osaka Prefecture University in 2002 and 2004. She joined NEC Corporation in 2004. She worked on research and development of a highly sensitive receiver for optical communication systems. In 2008, she joined the New Energy and Industrial Technology Development Organization (NEDO).

Tadayuki Chikuma received B.E. degrees from the Shinshu University in 1992. He joined NEC Corporation in 1992 and is now a manager in the NEC Yamanashi. He has been engaged in research and development on a highly sensitive receiver for optical communication systems.

Takeshi Takeuchi received his B.E. and M.E. degrees in physical electronics engineering from the Tokyo Institute of Technology in 1988 and 1990, respectively. Since he joined NEC Corporation in 1990, he has been engaged in the research and development of opto-electronic devices such as photo detectors and photonic integrated circuits. He is currently a engineer in Fiber Optics Device Division in NEC.

Kikuo Makita received his B.E., M.E., and Ph.D. degrees from Tohoku University in 1979, 1981, and 1998. He joined NEC Corporation. He has been engaged in research and development on a highly sensitive receiver for optical communication systems. He also has been a visiting professor in the Faculty of Science and Engineering, the Ritsumeikan University. Dr. Makita is a member of the Japan Society of Applied Physics and the Institute of Electronics, Information, and Communications Engineers of Japan. In 2010, he joined the Advanced Industrial Science and Technology (AIST).